

CLAIMS

What is claimed is:

- Sus A7*
1. A method of manufacturing a semiconductor device, wherein the method comprises:  
forming a final layer of metal on a layer of interlayer dielectric in the semiconductor device;  
forming a layer of TiN on the final layer of metal;  
forming a first layer of photoresist on the layer of TiN;  
patterning and developing the first layer of photoresist exposing portions of the 10 layer of TiN;  
etching holes in the layer of TiN and the final layer of metal exposing portions of the interlayer dielectric, wherein metal structures are formed; and  
removing the first layer of photoresist and the layer of TiN.
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- 15 2. The method of Claim 1 further comprising forming a blanket layer of interlayer dielectric on the surface of the semiconductor device.
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- Sus A2 7*
- 20 3. The method of Claim 2 further comprising:  
forming a second layer of photoresist on the blanket layer of interlayer dielectric;  
and  
patterning and developing the second layer of photoresist exposing portions of the blanket layer of interlayer dielectric overlying metal structures; and  
etching the exposed portions of the blanket layer of interlayer dielectric down to the metal structures.
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- 25 2. 4. The method of Claim 3 further comprising removing the second layer of photoresist.
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3. 5. The method of Claim 1 wherein the first layer of photoresist and the layer of 30 TiN is etched by a process utilizing fluorine containing gas chemistry at an elevated temperature.